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best options to review.

Digital design Q. 5.10: A sequential circuit has two JK flip flops A and B, two inputs x and y; and one output z *DIGITAL SYSTEM DESIGN OVERVIEW* Q. 5.6: A sequential circuit with two D flip-flops A and B, two inputs, x and y; and one output z is *Digital Design: Q. 1.13: Do the following conversion problems: (a) Convert decimal 27.315 to binary* Digital Design: Q. 1.10: Convert the following binary numbers to hexadecimal and to decimal: (a), (b Q. 7.7: A 16K * 4 memory uses coincident decoding by splitting the internal decoder into X - selection Q. 4.35: Implement a full adder with two 4 * 1 multiplexers.

Q. 1.1: List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digitsQ. 4.14: Assume that the

exclusive OR gate has a propagation delay of 10 ns and that the AND or OR **What Is Digital Design? - Deepend**

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adders (HDL—see Problem 4.54), (a) Design a full-subtractor circuit incremen Q. 5.1: The D latch of Fig. 5.6 is constructed with four NAND gates and an inverter. Consider the Lecture 4: Digital Logic Gates

Revised worksheet *Lecture 9: NAND and NOR (Universal Gates) Implementation*

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